A Comparison of Multilevel "Zero Inductor-Voltage" Converters for Data Center Applications

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***Abstract*—Datacenter power architectures have improved over time, but the majority of the loss still occurs at the server power supply and board level voltage regulators. Google has proposed and implemented a 48 volt server architecture that can reduce their overall conversion losses by up to 30%, but to fully realize these benefits new technology is needed to converter 48 volts down to the point of load voltage levels. The Intermediate Bus Architecture is a very attractive option to bridge the gap between the 48 volt architecture of cutting edge servers, and the existing 12 volt architecture. The family of converters presented in this paper are intermediate bus converters that have demonstrated up to 990W/in^3 power density, and higher than 99% peak efficiency for 48V to 12V conversion. Compared with other cutting edge designs this family of converters achieves high power density and efficiency without the need for complex control, or a sensitive resonant based design. This is achieved through low reliance on magnetic components, without the drawbacks traditionally associated with switched capacitor topologies.**

Keywords— DC-DC converter, bus converter, 48V to 12V, step-down converter, data center, Zero Inductor-Voltage

I. Introduction

Data centers and servers are one of the largest growing consumers of electrical power in the world today. In 2017 there were 8.4 billion "internet of things" connected devices. This is expected to rise to over 20 billion devices by 2020, as over 1 billion new internet users are expected to emerge during that time, growing from 3 billion to over 4 billion [1]. Data center architecture has evolved over time, and significant gains have been realized at the building level power conversion steps, however, the majority of the loss still occurs at the server PSU and board-level voltage regulators. As shown in Table 1, efficiencies significantly above 90% have been achieved at the UPS and PDU stages, but the server power supply unit, and point of load voltage regulators have relatively low efficiency, often well below 90%. Google's approach has been to implement what they refer to as a 48 volt power architecture [4]. Google has estimated that this change can reduce their conversion losses 30%, as well as offering a 16x reduction in the distribution losses throughout the rack [5]. However, this 48 volt to POL conversion can be very challenging, particularly for low voltage high current loads such as modern processors. The most common approach is to utilize a two-stage conversion approach, such as the Intermediate Bus Architecture, to achieve this stepdown at high efficiency [6][7]. The family of converters presented in this paper are intermediate bus converters aimed at 48 volt datacenter applications.

II. Topology Overview

A. 7-Switch Zero Inductor-Voltage Converter

The 7-Switch Zero Inductor-Voltage (ZIV) Converter, introduced in [8] and shown in Figure 1, has many attractive features for use as a bus converter. As a multilevel topology, the 7-Switch ZIV converter reduces the voltage stress of the individual MOSFETs and capacitors, allowing for significantly improved performance, and a reduction in converter size. Additionally, the "zero inductor-voltage" property, as outlined in [8] allows for a very small output inductor to be used even at low switching frequency, as the output filter only needs to filter the capacitor ripple to produce a DC output. Similar to a switch capacitor converter topology, this can result in significant improvements in power density and efficiency compared with conventional topologies that are highly reliant on magnetic components, but unlike a switched capacitor converter the ZIV converter does not have any issue associated with the paralleling of large flying capacitors. This means there are no current spikes and charge-redistribution loss associated with the switching operation of the converter. This is illustrated in Figures 2-4, which show the 3 operating states of the 7-Switch ZIV converter. As shown in Figures 2-4, the capacitors are always connected in series. This is a significant advantage as traditional switched-capacitor converter topologies must use either very large capacitors, or high switching frequencies, to minimize the

TABLE I. Efficiency of Power Conversion Steps in Data Centers [2][3]

Architecture	Efficiency					
	UPS	***PDU***	***Rack-Level***	***Server PSU***	***VR Stage***	***Overall***
Traditional AC	89.2%	93.2%	N/A	75.5%	81.6%	51.6%
High-Efficiency AC	97.1%	94.0%	N/A	88.0%	87.7%	69.9%
Rack-Level 48VDC	97.1%	93.8%	92.4%	91.5%	87.7%	67.4%
Facility-Level 400VDC	95.3%	96.8%	N/A	89.1%	87.7%	72.7%

losses associated with charge redistribution, resulting in a trade-off between power density and efficiency that the ZIV converter avoids. In the ZIV converter, inductors as small as 100nH can be used even for switching frequencies below 100kHz. In this way, the ZIV converter maintains the key benefits of the switched capacitor converters, namely the low reliance on bulky magnetics, while avoiding one of the critical drawbacks.

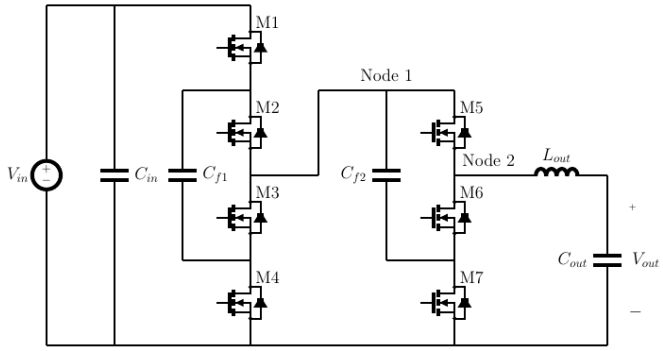

Fig. 1. 7-Switch ZIV Converter Topology

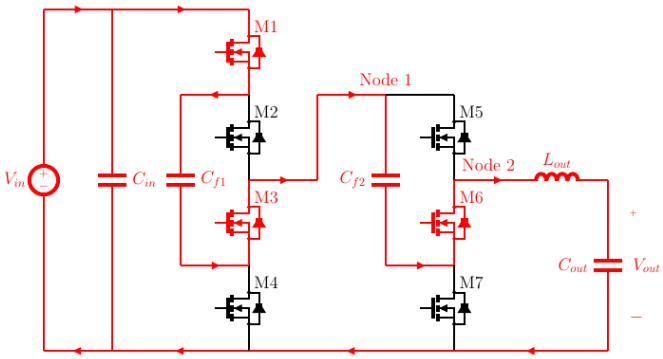

Fig. 2. 7-Switch ZIV Converter Operating State A

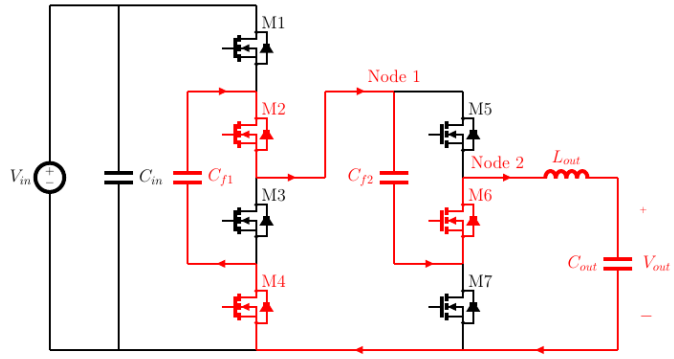

Fig. 3. 7-Switch ZIV Converter Operating State B

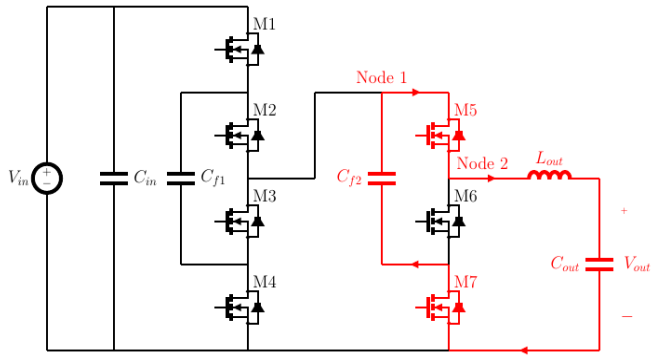

Fig. 4. 7-Switch ZIV Converter Operating State C

B. Multiphase ZIV Converters

Along with efficiency and power density, scalability is one of the other key criteria for an effective bus converter topology. Utilizing multiple phases in parallel is an extremely effective option to achieve higher output power in a straight-forward, modular way. For bus converters, the output voltage is typically not regulated. This can create potential problems, as the lack of control makes it difficult to ensure even current sharing in certain topologies. In the case of the ZIV converter, multiphase operation with good current sharing can be achieved passively as discussed in [9]. According to the measurements presented in Figure 5, the ZIV converter's output voltage decreases as the output current increases. As demonstrated by other bus converter topologies, such as the switched tank converter [11], this property allows for good droop current balancing to be achieved with a symmetrical layout and with no active control required.

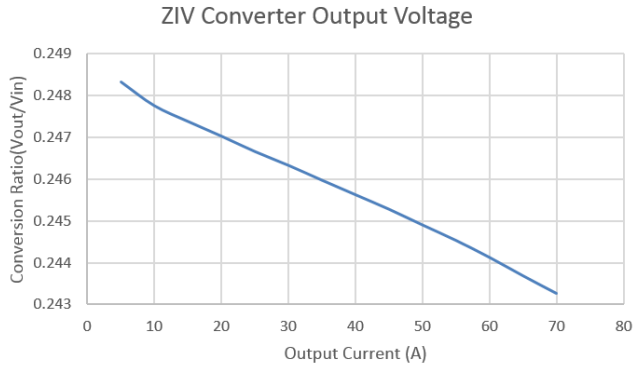

Fig. 5. ZIV Converter Conversion Ratio vs Output Current

In a multiphase ZIV converter, there is an additional key advantage offered by utilizing multiple phases, rather than a single 7-switch ZIV converter. In the ZIV converter, the first-stage MOSFETs (M1-M4) operate at 25% duty cycle. As discussed in [8] this results in relatively large input capacitor RMS current. As this input capacitor also has a voltage stress that is two or four times higher than any of the other components, in the 7-Switch ZIV converter the input capacitor is one of the largest components on the board, requiring a large number of ceramic capacitors in parallel to achieve low ESR to minimize the loss, as well as providing a sufficiently large capacitance value at the input. In a multiphase ZIV converter,

however, the phases can be operated with a relative phase-shift. In the example of a two-phase ZIV converter [9] the two phases can be operated with a 180 degrees phase shift, as shown in Figure 6.

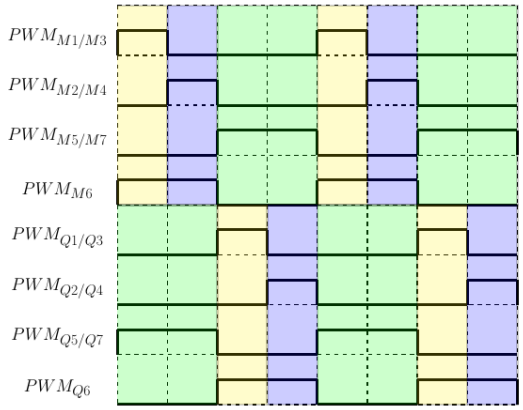

Fig. 6. Two-Phase ZIV Converter Gate Drive PWM Diagrams

This increases the effective duty cycle seen by the input capacitor to 50%, reducing the RMS current losses by a factor of 3. This allows for a significant reduction in capacitor size, and associated losses. Furthermore, using a four-phase ZIV converter, the input capacitor could be almost entirely eliminated through this interleaving operation. This means that multiphase operation for the ZIV converter not only provides the key advantage of scalability, but additionally improves the performance of the converter in terms of both efficiency and power density when compared with a single 7-Switch ZIV converter.

C. 12-Switch ZIV Converter

The main disadvantage of the two ZIV converter topologies presented above is that the first stage MOSFETS operate with only a 25% duty cycle. From a device utilization perspective, it would be advantageous to operate the first stage MOSFETs at 50% duty cycle to improve the performance of the converter. To achieve this the 12-Switch ZIV converter topology, presented in [10] was developed. The converter topology is shown in Figure 7. The operation of the 12-Switch ZIV converter can be most easily understood by examining the operation of a Two-Phase ZIV converter, in particular the PWM gate diagram shown in Figure 6. As shown in Figure 6 the first phase input stage is inactive for 50% of the overall converter switching period, while the second phase input stage is operating. It is therefore possible to combine these two separate input stages into a single stage, operating with 50% duty cycle at twice the frequency of the two output stages. This results in the topology shown in Figure 7. It should be noted however, that in the case of the 12-Switch ZIV converter topology a switch must be added to each of the output stages. This switch is necessary because the voltage at Node 1 can no longer be allowed to be pulled down to the output voltage during the operating state shown in Figure 4. However, compared with a true Two-Phase ZIV converter the 12-Switch ZIV converter utilizes two fewer MOSFETs and, more significantly, eliminates one flying capacitor for the same output power capability. As detailed in [10] the 12-Switch ZIV converter, compared with a Two-Phase ZIV converter, achieves very similar overall efficiency, with the only efficiency penalty coming from the addition of MOSFETs Q5 and M5.

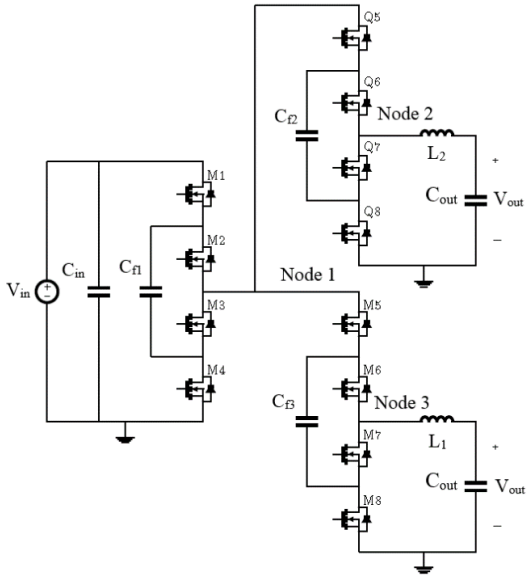

Fig. 7. 12-Switch ZIV Converter Topology

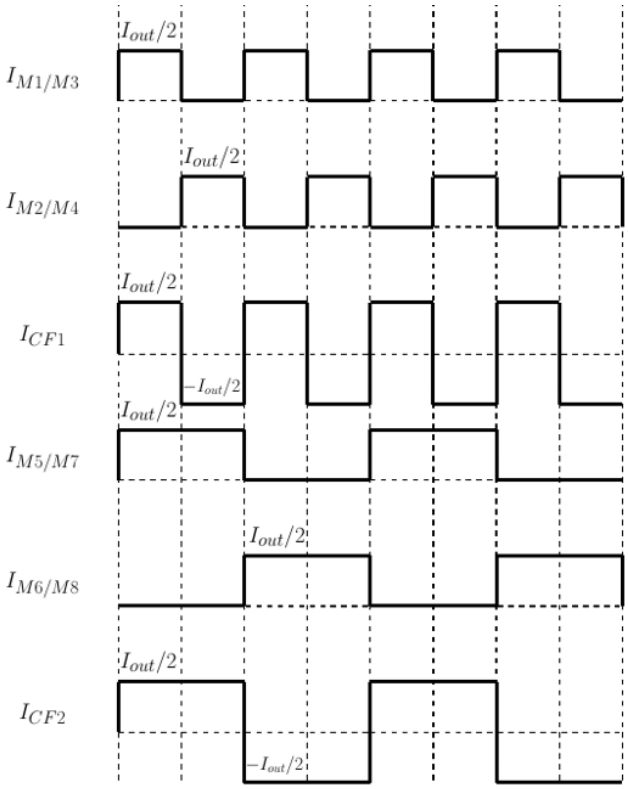

Fig. 8. Approximate Current Waveforms for the 12-Switch ZIV Converter (M1-M8 "phase")

Figure 8 shows the approximate current waveforms for one "phase" of the 12-Switch ZIV converter consisting of M1-M8. From these waveforms it can be more clearly understood how the 12-Switch ZIV converter achieves very similar efficiency performance to the Two-Phase ZIV Converter. First, while the switching frequency of the first stage (M1-M4) is doubled, the number of devices is halved. For the second stages, the operation is equivalent to the Two-Phase ZIV converter with the addition of two high-side MOSFETs (M5 and Q5). Therefore the total switching related loss is not increased by the higher frequency of the input stage, but only due to the addition of the two MOSFETs in the second stage. More importantly, as the conduction loss is the dominant source of loss in the ZIV converter topology [8], the 12-Switch ZIV converter achieves the same overall conduction loss as the Two-Phase ZIV converter for the input stage due to the improved utilization of the MOSFETs that are now operating at 50% duty cycle. In a Two-Phase ZIV converter the input stage MOSFET current stress for each of the 8 MOFETs is given by:

$$I_{RMS} = \sqrt{0.25}\frac{I_{out}}{2} \qquad (1)$$

For the 12-Switch ZIV converter the MOSFET current stress for each of the 4 input MOSFETs is:

$$I_{RMS} = \sqrt{0.5}\frac{I_{out}}{2} \qquad (2)$$

The conduction loss per MOSFET for the Two-Phase ZIV converter is then:

$$P_{cond} \approx \frac{I_{out}^2}{16} \qquad (3)$$

For the 12-Switch ZIV converter:

$$P_{cond} \approx \frac{I_{out}^2}{8} \qquad (4)$$

Noting that the Two-Phase ZIV converter has 8 devices compared with only 4 for the 12-Switch ZIV converter it is then clear that the overall conduction loss for the input stage is equal for both topologies. Analyzing the flying capacitor currents produces the same result. As with the switching loss comparison the operation of the two output stages is equivalent, with the addition of M5 and Q5 being the only additional sources of loss. Therefore, as is verified in the Experimental Results, the 12-Switch ZIV converter achieves a higher power density through a component count reduction, with only a small overall impact on the efficiency of the converter, making it an attractive option for high density applications such as in data center power supplies.

III. Loss Breakdown

The loss breakdowns for the three ZIV converter topologies are presented in Figures 9, 10 and 11. This analysis is conducted using identical MOSFET, inductor and capacitor parameters with a switching frequency of 60kHz. For the 7-Switch ZIV converter the analysis is presented for 25A output load, and for both the 12-Switch and Two-Phase ZIV converters the analysis is done with 50A output load.

A. 7-Switch ZIV Converter

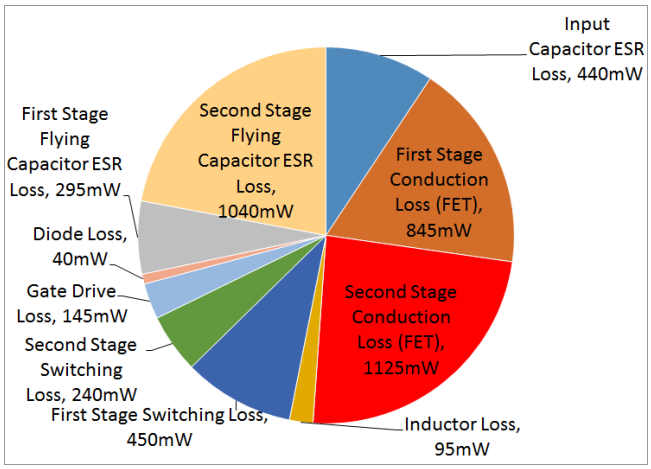

Fig. 9. 7-Switch ZIV Converter Loss Analysis (50A Load, 60kHz)

For the 7-Switch ZIV converter the dominant sources of loss are the conduction losses in both the MOSFETs and flying capacitors. This is due largely to the very low frequency operation of the converter, coupled with the low voltage stress of the MOSFETs allowing for the switching losses to be minimized even in a hard-switching converter topology.

B. Two-Phase ZIV Converter

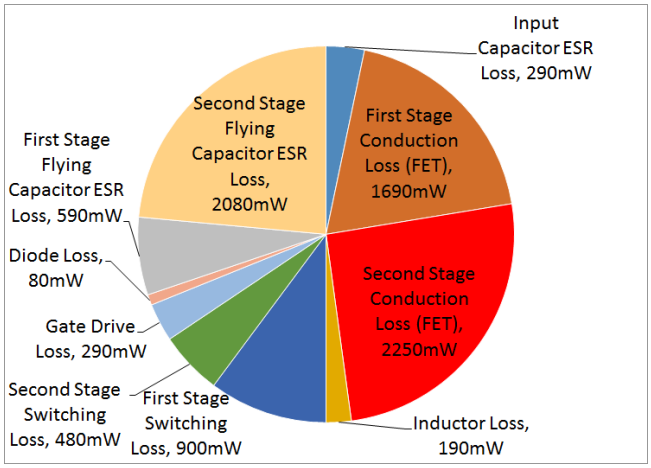

Fig. 10. Two-Phase ZIV Converter Loss Analysis (50A Load, 60kHz)

As expected, the two-phase ZIV converter loss is simply double that of the 7-Switch ZIV converter, for double the output current, with the notable exception of the input capacitor. Due to the interleaving of the input capacitor the ESR loss associated with this component is reduced in the Two-Phase ZIV converter, resulting in higher overall efficiency.

C. 12-Switch ZIV Converter

In the 12-Switch ZIV converter the loss is very similar to the Two-Phase ZIV converter, with the only additional sources of loss being M5 and Q5 adding to the second stage switching losses, and second stage conduction losses of the converter.

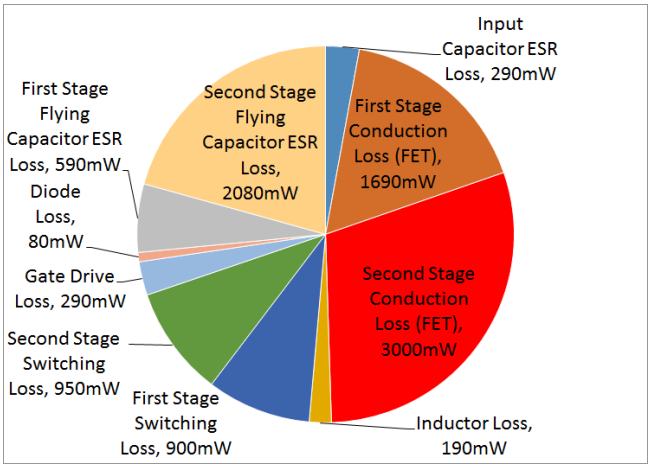

Fig. 11. 12-Switch ZIV Converter Loss Analysis (50A Load, 60kHz)

IV. Experimental Results

Experimental results are presented for the Two-Phase ZIV converter and 12-Switch ZIV converter. Results from the 7-Switch ZIV converter presented in [8] are not included as, as shown in Figure 14, this prototype is much larger, utilizing several different components which prevents a direct and fair comparison from being made. For comparisons involving the 7-Switch ZIV converter simply one phase of the Two-Phase ZIV converter prototype is utilized to provide a direct comparison utilizing the same components. The two prototypes shown in Figures 12 and 13 utilize the components outlined in Table 2. The efficiency comparison for the three converter topologies, all operating at a base switching frequency of 60kHz (therefore 120kHz for the input stage FETs of the 12-Switch ZIV converter) is presented in Figure 15. The power densities of the three topologies are 750W/in^3 for the 7-Switch ZIV converter, 800W/in^3 for the Two-Phase ZIV converter, and 990W/in^3 for the 12-Switch ZIV converter prototypes. Due to the higher input capacitor ESR losses, the 7-Switch ZIV converter achieves slightly lower efficiency than the Two-Phase ZIV converter at equivalent per-phase current levels (97.8% vs 97.9% at full load of 35A per phase). However, the 7-Switch ZIV converter achieves superior performance at very light load, due primarily to the reduction in the gate drive losses, which are proportional to the number of MOSFETs rather than the load current.

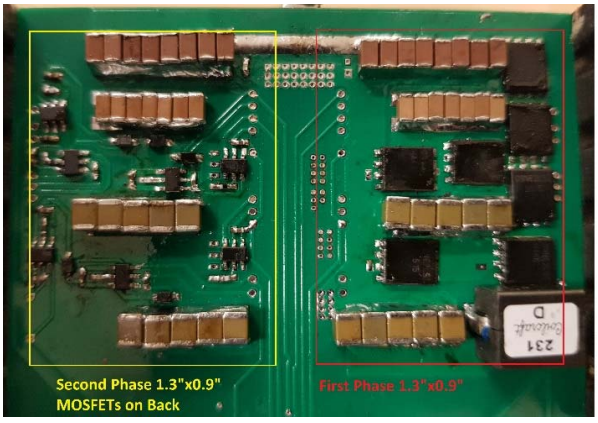

Fig. 12. Two-Phase ZIV Converter Prototype

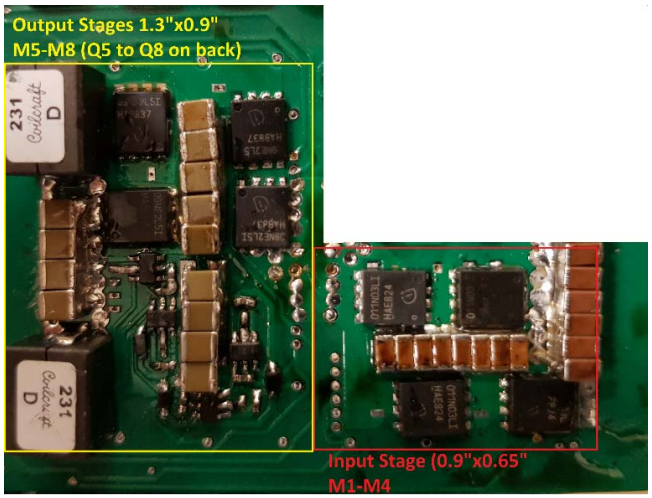

Fig. 13. 12-Switch ZIV Converter Prototype

Fig. 14. Size Comparison for Two-Phase ZIV Converter Prototype versus early 7-Switch prototype in [8]

TABLE II. PROTOTYPE COMPONENTS

Prototype Components	*Two-Phase*	*12-Switch*
First Stage FET	30V BSC011N03LSI	30V BSC011N03LSI
Second Stage FET	25V BSC009NE2LS5I	25V BSC009NE2LS5I
First Stage Capacitor	14x10uF 50V JB 1206	16x10uF 50V JB 1206
Second Stage Capacitor	10x47uF 25V X5R 1210	9x47uF 25V X5R 1210
Input Capacitor	15x4.7uF 100V X7S 1210	15x4.7uF 100V X7S 1210
Output Capacitor	12x47uF 25V X5R 1210	12x47uF 25V X5R 1210
Inductor	230nH SLR1075-231KE	230nH SLR1075-231KE
Switching Frequency	60kHz	120kHz (first stage) 60kHz (second stage)

Therefore, based on these experimental results the 7-Switch ZIV converter is the best choice for very light loads only, with the multi-phase and 12-Switch ZIV converter topologies offering significant performance improvements in both

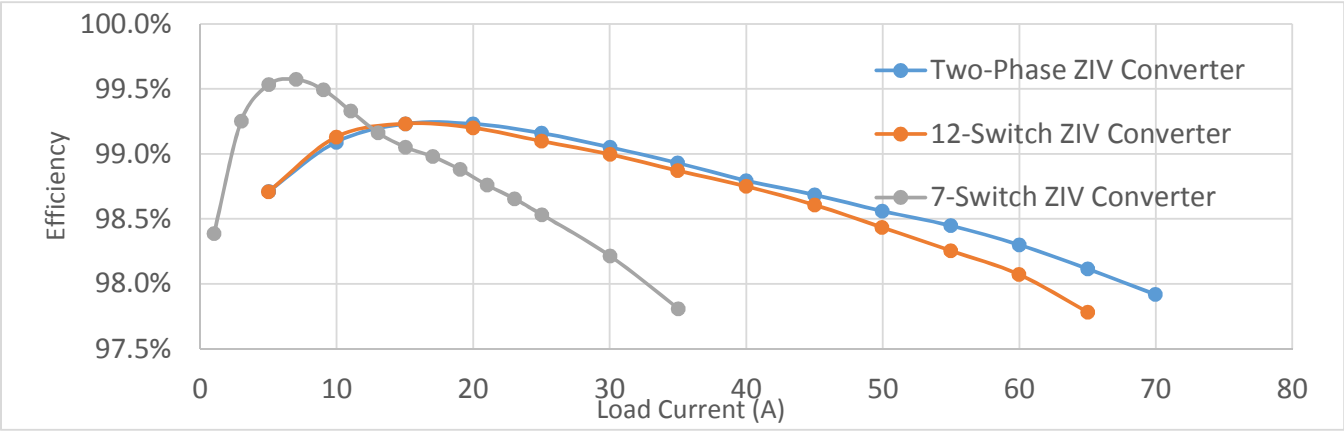

Fig. 15. Efficiency Measurements

efficiency and power density at higher loads. As expected, from the loss analysis, the 12-Switch ZIV converter has only a small efficiency penalty when compared with the Two-Phase ZIV converter, primarily at heavier loads, which also achieving approximately 25% better power density due to the reduction in overall component count.

Figure 16 below shows the input voltage, voltage at the node connecting the input and output stages (Node 1 in Figure 1) and the output voltage for one phase of the two-phase ZIV converter prototype operating at 30A load. Figure 17 shows the same voltages, input, Node 1 and output, for the 12-Switch ZIV converter. Note that the addition of MOSFETs M5 and Q5

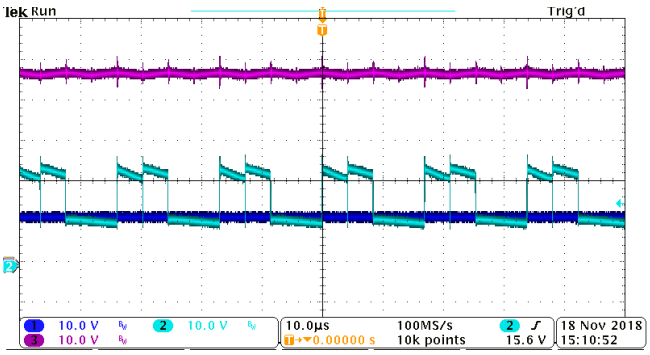

Fig. 16. Input Voltage, Node 1 Voltage, Output Voltage Two-Phase

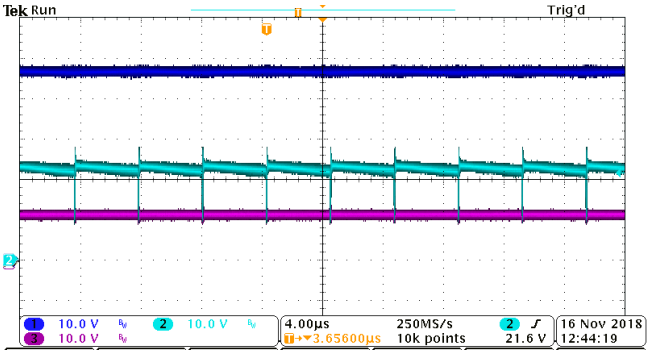

Fig. 17. Input Voltage, Node 1 Voltage, Output Voltage 12-Switch

successfully prevent the Node 1 voltage from being pulled down to the output voltage during the operation of the converter. Figure 18 shows the Node 2 voltage for one phase of the Two-Phase ZIV converter prototype operating at 30A load. This figure demonstrates the zero inductor-voltage property for which this converter family is named; the output voltage at Node 2 is equal to the DC output voltage with only some capacitor ripple. This is the key operating principle, first presented in [8] that enables these converter topologies to use extremely small inductors at very low switching frequency to achieve high power density and efficiency. Figure 19 presents the Node 2 and Node 3 voltages for the 12-Switch ZIV converter at the same load condition, verifying that in this topology the ZIV property is maintained.

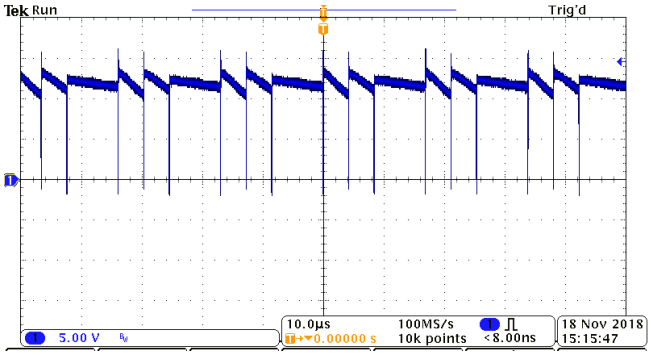

Fig. 18. Node 2 Voltage Two-Phase

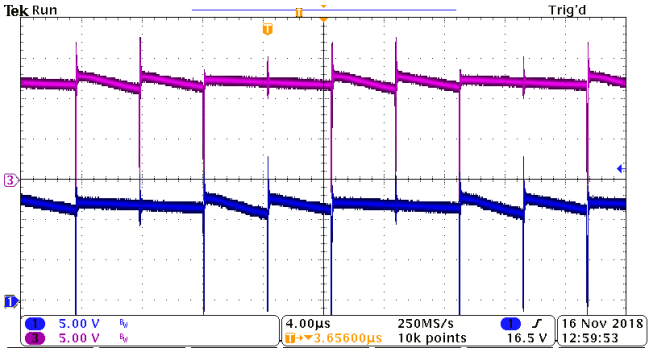

Fig. 19. Node 2 and Node 3 Voltages 12-Switch

While the efficiency measurements presented in Figure 15 provide evidence that sufficiently good current sharing performance is achieved at steady state for both the Two-Phase ZIV converter and 12-Switch ZIV converter, to further verify the steady state current sharing thermal images of both prototypes are provided. The thermal images are taken for the Two-Phase ZIV and 12-Switch ZIV converters operating at 35A load current with no external cooling. Figures 20 and 21 show the first and second phases for the Two-Phase ZIV converter, while Figures 22 and 23 show the two output stages of the 12-Switch ZIV converter. As expected, both converters show similar operating temperatures between their respective phases, indicating that even current sharing is achieved passively by the two converter topologies. It is also expected that the 12-Switch ZIV converter reaches a slightly higher temperature for the same output load condition, as while the overall loss is increased only slightly, the component count is lower resulting in higher temperature of the individual components.

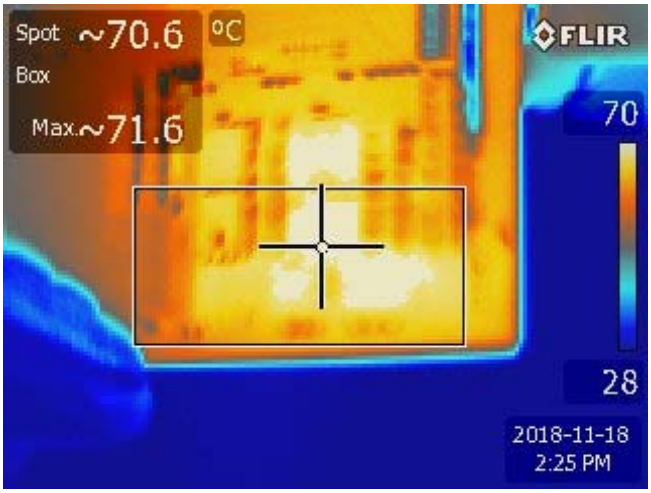

Fig. 20. Two-Phase ZIV Converter Thermal Performance, No Cooling

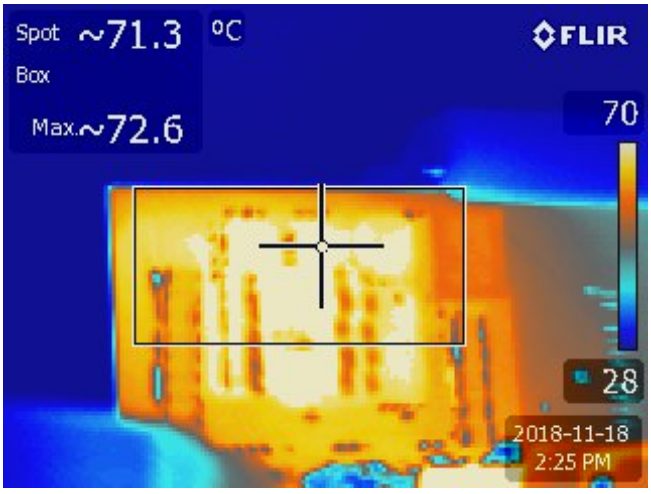

Fig. 21. Two-Phase ZIV Converter Thermal Performance, No Cooling

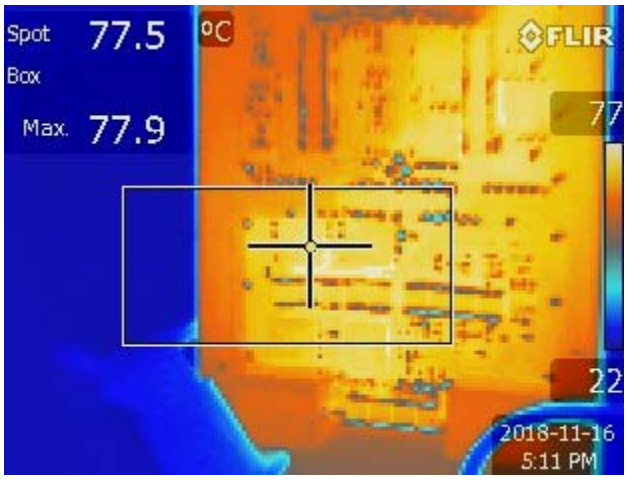

Fig. 22. 12-Switch ZIV Converter Thermal Performance, No Cooling

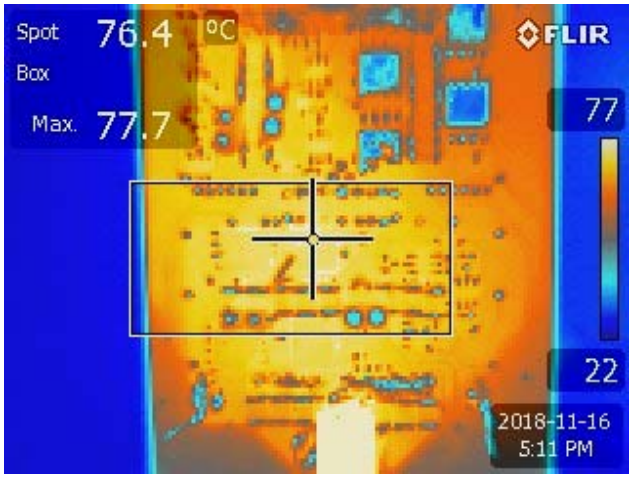

Fig. 23. 12-Switch ZIV Converter Thermal Performance,No Cooling

V. Conclusions

A family of power converters aimed at 4:1 stepdown bus converter applications has been presented. This family of converters is capable of achieving extremely high power density, and efficiency owing largely to its multilevel structure, and the zero inductor-voltage property for which it is named. Similar to a switched-capacitor converter, the ZIV converters are able to achieve very low reliance on magnetic components in order to improve overall efficiency and power density. However, unlike traditional SC converters, the ZIV converter family never places the flying capacitors in parallel, eliminating the issue of the current spikes that occur in traditional SC topologies. A 4:1 stepdown Dickson SC converter is presented in [12] for 48V to 12V bus converter applications. Due to the inherent advantages of the ZIV converter topology over traditional SC topologies, such as the Dickson converter, the ZIV converter demonstrates far higher efficiency and power density. Other topologies, such as Google's Switched Tank converter [11] attempt to utilize the principles of SC converter topologies to achieve similarly high efficiency and power density.

TABLE III. PERFORMANCE METRICS FOR SELECTED BUS CONVERTER TOPOLOGIES

Converter Topology	Performance Metrics					
	Power Density	***Peak Efficiency***	***Full-Load Efficiency***	***# of Switches***	***# of Flying Capacitors***	***Output Power***
7-Switch ZIV	750W/in^3	99.5%	97.8%	7	2	420W
Two-Phase ZIV	800W/in^3	99.2%	97.9%	14	4	840W
12-Switch ZIV	990W/in^3	99.2%	97.8%	12	3	780W
Dickson SC [12]	400W/in^3	98.0%	96.9%	10	3	500W
Switched Tank [11]	500W/in^2	98.6%	97.4%	10	3	650W (13.5V output)

This Switched Tank topology, and other similar topologies [13-19] commonly utilize added inductors to prevent the current spikes associated with the paralleling of the flying capacitors. In some topologies, such as the Switched Tank converter, these added inductors also allow resonant operation to be achieved. However, as indicated in Table 3, while the Switched Tank converter achieves notable improvements over a traditional SC converter topology, the efficiency is lower than the ZIV converter family. Additionally, the Switched Tank converter and other similar converters must make use of a more complex resonant design. While the Switched Tank converter is able to utilize capacitors with inherently lower component tolerances, many of these Switched Capacitor based topologies that utilize additional inductors are highly sensitive to component non-idealities [11] preventing their widespread adoption. The ZIV converter family does not rely on resonant operation, and therefore is essentially immune to component variations; any component non-idealities will simply change the capacitor votlage ripple, or inductor current ripple by a small amount which does not largely impact the converter operation.

In conclusion, the ZIV converter family demonstrates extremely high efficiency and power density, competitive with or superior to other cutting-edge bus converter topologies. With a peak efficiency above 99%, full load efficiency of nearly 98%, and up to nearly 1kW/in^3 power density, the ZIV converter family achieves excellent performance in all of the most important criteria by which bus converter topologies are evaluated. In addition to excellent performance, the ZIV converter family is a simple design that does not rely on sensitive resonant operation and is largely immune to component non-idealities.

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